Homework 1

(Due date: January 24th @ 5:30 pm)
Presentation and clarity are very important!

PROBLEM 1 (25 PTS)

a) Simplify the following functions using ONLY Boolean Algebra Theorems. For each resulting simplified function, sketch the logic circuit using AND, OR, XOR, and NOT gates. (9 pts)

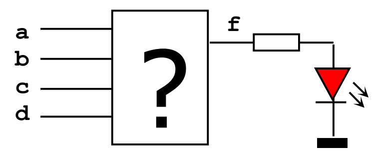
✓ $F = A(C + \bar{B}) + \bar{A}$ ✓ $F = (Y + Z)(\bar{Y} + X)$ ✓ $F(X, Y, Z) = \prod(M_0, M_1, M_4, M_5)$

b) For the following Truth table: (6 pts)

- Provide the Boolean function using the Canonical Sum of Products (SOP), and Product of Sums (POS).
- Express the Boolean function using the minterms and maxterms representations.
- Sketch the logic circuit as Canonical Sum of Products and Product of Sums.

x	y	z	f
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

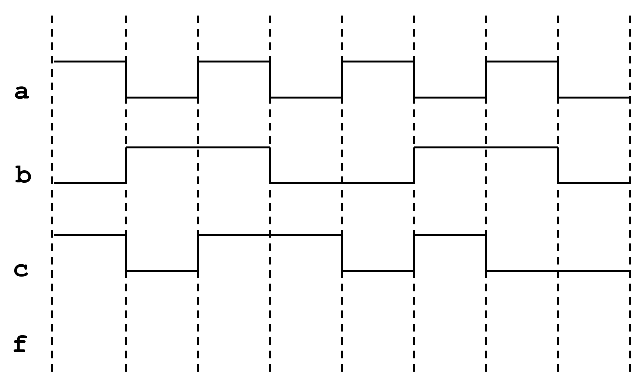
c) Complete the truth table for a circuit (active high inputs, active high outputs) that activates an output (f='1') when the decimal value of the 4 inputs is equal to 0, 3, 5, 6, 9, 12, or 13. Then, simplify the function using Karnaugh maps. (10 pts)



PROBLEM 2 (15 PTS)

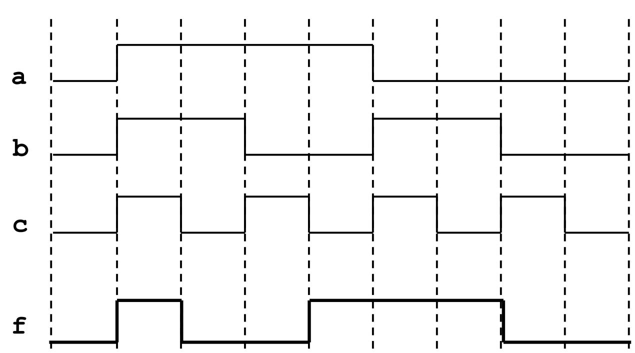
a) Complete the timing diagram of the logic circuit whose VHDL description is shown below: (5 pts)

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
  port ( a, b, c: in std_logic;
         f: out std_logic);
end circ;

architecture st of circ is
  signal x, y: std_logic;
begin
  x <= a and b;
  y <= x nand c;
  f <= y xor (not b);
end st;
```



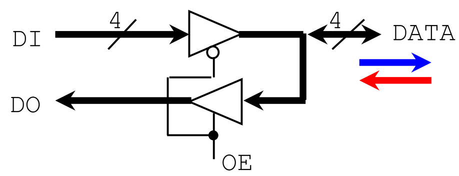
b) The following is the timing diagram of a logic circuit with 3 inputs. Sketch the logic circuit that generates this waveform. Then, complete the VHDL code. (10 pts)

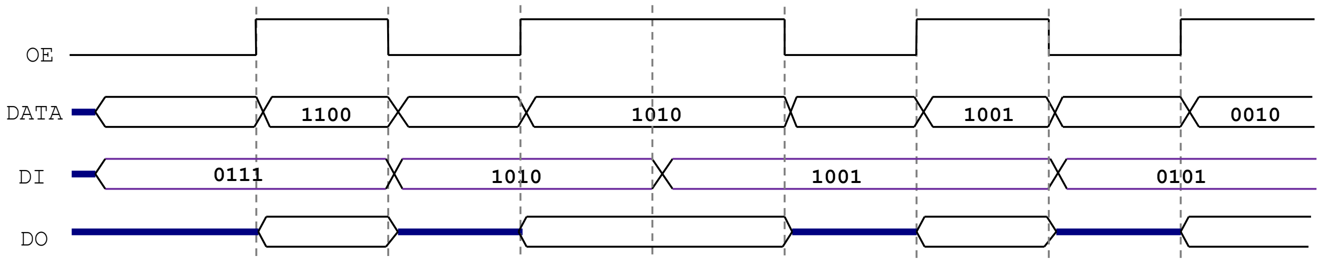
```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
 port ( a, b, c: in std_logic;
        f: out std_logic);
end circ;

architecture st of circ is
-- ???
begin
-- ???

end st;
```



PROBLEM 3 (10 PTS)

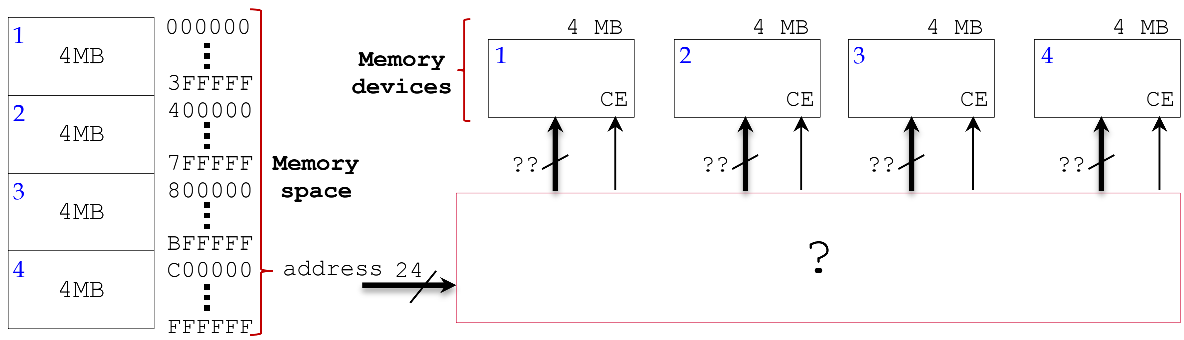
- For the following 4-bit bidirectional port, complete the timing diagram (signals DO and $DATA$):





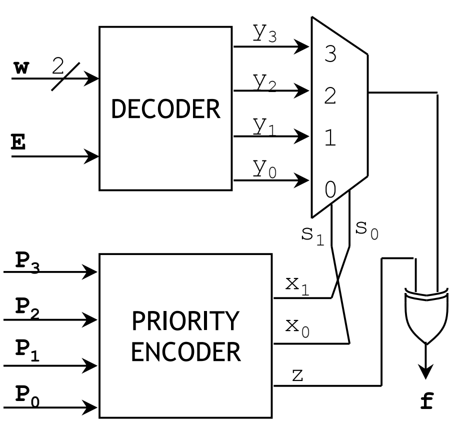
PROBLEM 4 (10 PTS)

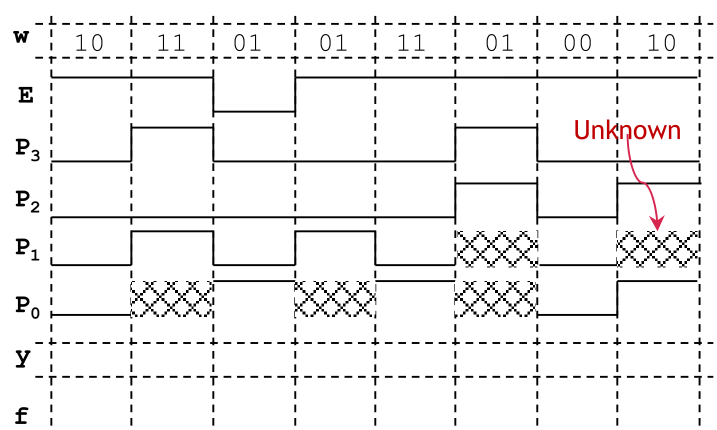
- A 24-bit address line in a μprocessor handles up to $2^{24} = 16\ MB$ of addresses, each address containing one-byte of information. We want to connect four 4MB memory chips to the μprocessor.
- Sketch the circuit that: i) addresses the memory chips, and ii) enables only one memory chip (via CE: chip enable) when the address falls in the corresponding range. Example: if $address = 0x5FFFFF$, → only memory chip 2 is enabled (CE=1). If $address = 0xD00FA0$, → only memory chip 4 is enabled.
- Complete the number of bits '??' required for each 4MB memory chip.



PROBLEM 5 (15 PTS)

- Complete the timing diagram of the circuit shown below:





PROBLEM 6 (15 PTS)

- In these problems, you MUST show your conversion procedure.

a) Convert the following unsigned integer numbers to their binary and hexadecimal representation. (4 pts)
124, 115, 128, 255.

b) What is the minimum number of bits required to represent: (3 pts)
✓ 50,000 colors?
✓ 32679 symbols?
✓ 65536 memory addresses in a computer?

c) A microprocessor can handle addresses from `0x0000` to `0x1FFF`. How many bits do we need to represent those addresses? (2 pts).

d) Complete the following table. (6 pts)

Decimal	BCD	Binary number	Reflective Gray Code
128			
		10101011	
	0100 1001		
			10001001
		1110010	
	0110 0011 0001		

PROBLEM 7 (10 PTS)

- Complete the timing diagram of the digital circuit shown in the figure below. You must consider the propagation delays. Assume that the propagation delay of every gate is 5 ns. The initial values of the signals are specified in the figure.